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REDUCTION OF LEAKAGE BY INPUT VECTORS WITH CONSTRAINED NBTI DEGRADATION

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Technology scaling has caused Negative Bias Temperature Instability (NBTI) to emerge as a major circuit reliability concern for the circuit designers Simultaneously leakage power is becoming a greater fraction of the total power dissipated by logic circuits. As both NBTI and leakage power are highly dependent on vectors applied at the circuit's inputs, they can be minimized by applying carefully chosen input vectors during periods when the circuit is in standby or idle mode. Unfortunately input vectors that minimize leakage power are not the ones that minimize NBTI degradation, so there is a need for a methodology to generate input vectors that minimize both of these variables. This paper proposes such a systematic methodology for the generation of input vectors which minimize leakage power under the constraint that NBTI degradation does not exceed a specified limit. These input vectors can be applied at the primary inputs of a circuit when it is in standby/ idle mode and are such that the gates dissipate only a small amount of leakage power and also allow a large majority of the transistors on critical paths to be in the "recovery" phase of NBTI degradation.

The advantage of this methodology is that allowing circuit designers to constrain NBTI degradation to below a specified limit enables tighter guardtbanding, increasing performance. Constrain of NBTI can be limited by choosing input vectors probability based algorithms. Our methodology guarantees that the generated input vector dissipates the least leakage power among all the input vectors that satisfy the degradation constraint. We formulate the problem as a zero-one integer linear program and show that this formulation produces input vectors whose leakage power is within 1% of a minimum leakage vector selected by a search algorithm and simultaneously reduces NBTI by about 5.75% of maximum circuit delay as compared to the worst case NBTI degradation.

Keywords: NBTI, Leakage, Input Vector, Critical Path

1. Introduction

Relentless technology scaling has caused Negative Bias Temperature Instability (NBTI) to emerge as a major concern for circuit reliability. NTBI occurs when PMOS transistors are negatively biased, (i.e.$Vgs = -V_{DD}$) at elevated temperature causing a shift in the threshold voltage (Vth).Over a long period of time, such accumulated shifts can cause a significant increase the delay of these transistors, resulting in a degradation of the circuit's operating frequency. A number of techniques have been proposed to combat the effects of NBTI degradation, such as gate sizing [4, 11], adaptive body biasing [5], adjustment of supply voltage, signal probability etc. [8] and bit flipping [2]. The reduction of leakage power is also an important design goal in modern technologies. A popular method for leakage power reduction is Input Vector Control (IVC) [1, 13]. The basic idea behind this method is that when the circuit is idle or sleeping, input vectors which dissipate minimal leakage power are applied. The technique is effective because there is a significant difference in the leakage power dissipated by different input vectors. The technique of input vector control (IVC) is attractive from the point of view combating NBTI degradation as well because IVC can mitigate the impact of NBTI over and above the effect of techniques like gate sizing. The reduction of leakage power is also an important design goal in modern technologies. The basic idea behind IVC is to apply an input vector such that a large number of the PMOS transistors of the gates along the critical path of the circuit are not negatively biased (i.e. input value 1). Ideally we would like to have input value 1 at all points in the circuit, but this is not possible for real word circuits because the presence of logical negations implies that some values will necessarily be the complement of others. Thus the IVC problem for NBTI is to select an input vector that ensures that a large number of PMOS transistors are in recovery (i.e. receiving input 1) along the critical and near critical paths in the circuit. As noted in previous work [10], input vectors that minimize leakage power may not be the ones that minimize degradation. As a result it is necessary to select vectors that co-optimize leakage and NBTI degradation. In this paper, our approach is to select input vectors that minimize leakage power while simultaneously constraining the NBTI degradation that occurs due to that vector to be less than a certain value called the degradation limit. Thus, circuit designers can use the well known technique of guardbanding to design their circuits with the required amount of delay slack to account for delay degradation due to NBTI while simultaneously minimizing

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leakage power. Being able to limit NBTI degradation (for known values of gate input probabilities and utilization) gives designers a easy way to trade-off leakage power for performance, by allowing circuit designers to use a smaller degradation limit, (i.e. smaller guardband) in exchange for higher leakage power.

This paper makes the following contributions. We present a 0/1 ILP formulation that can be used to obtain the input vector that dissipates the minimum leakage power under the constraint that NBTI degradation does not exceed a certain factor. Although previous work [9, 10] has attempted to obtain input vectors that minimize both leakage power and NBTI degradation, these methods are not guaranteed to provide optimal solutions. Furthermore, these methods also do not provide a rigorous way of trading-off leakage power to limit NBTI degradation or vice versa. On the other hand, our method provides fine grained control over the trade-off between performance, reliability and power. Our results show that our formulation can produce input vectors that dissipate leakage power that is within 1% of that leakage power dissipated by an input vector generated by a search algorithm and simultaneously reduces NBTI degradation by 5.75% from the worst case. We show that our algorithms select an order of magnitude fewer paths as compared to previous work [7, 12]. The rest of the paper is structured as follows. Section II presents the NBTI degradation model that we assume in the rest of the paper. Section III develops the ILP formulation of the problem. Section IV presents evaluates our technique and Section V concludes.

2. NBTI Degradation Model

Vattikonda et al. [6] proposed a predictive NBTI degradation model for both static and dynamic NBTI.The dynamic NBTI model takes into account the recovery processes that mitigate the effect of NBTI degradation that occur when the reverse bias on the PMOS transistors is removed. They provide equations that model the change in N_{it}, the number of positive interface traps. These equations can be used to compute the change in N_{it} over the circuit's lifetime, from which we can derive the change in the threshold voltage-V_{th} and the corresponding delay degradation. The disadvantage of this model is that it is computationally expensive as -Vth degradation has to be calculated by simulation over the entire circuit lifetime. To mitigate this problem, a number of models [3, 7] have been proposed based on a curve-fitting approach to obtain a closed form approximation for -V_{th}. For the results presented in this paper, we use the model proposed by Luo et al. [3]. According to this model, the degradation in threshold voltage -V_{th} is given by the following equation.

$$V_{th} = \eta_0 . p^{0.27ps + 0.28s} . t^{1/4} \quad (1)$$

Where the coefficient η_0 is given by:

$$\eta_0 = ATox\sqrt{Cox(Vgs - Vth)\exp(Eox / E0)\exp(-Ea / kbT)} \quad (2)$$

We obtained the parameters in Equations 1, 2 for the 65-nm technology node from [6] and [14].It is well known that the delay of a gate g is given by the following equation:

$$D_g = \frac{\alpha V_{dd}}{(V_{dd} - Vth)_\beta} \quad (3)$$

We do not require the value of the constant as we interested in ratio of the degraded delay to the original delay of the gate. We note that our formulation is readily extensible to other NBTI degradation models, e.g. those that take into account the stacking effect.

3. Problem Formulation

We formulate this problem as an 0-1 Integer Linear Program (ILP).The variables of our ILP are the inputs and outputs of all the gates in the circuit and some additional variables that are added as described in the latter parts of this section. We have three types of constraints. One set of constraints express the input-output relation between gates. These are called the I/O constraints.A second set of constraints ensures that the maximum NBTI degraded delay of of the circuit does not increase beyond the degradation limit. We call these the path delay constraints. Finally, we have a third set of constraints called linearization constraints that are added for technical reasons. These convert a nonlinear integer program to an ILP. In the following subsections, we first show how to encode various aspects of the problem as a nonlinear integer program. In section III-D we show how to linearize the formulation using a well known transformation.

A. Modeling Leakage Power

Consider the example of a two input gate, with inputs x_1 and x_2. Let$\hat{}x_i$ be the value of input xi during sleep/standby mode. This value can be controlled by appropriately setting the primary inputs. We can model the leakage power dissipated by this gate using the following equation:

$$P(\hat{}x_1; \hat{}x_2) = c_0 + c_1 \hat{}\, x_1 + c_2 \hat{}\, x_2 + c_3 \hat{}\, x_1 \hat{}\, x_2 \quad (4)$$

There are four different values that $(\hat{}x_1;\hat{}x_2)$ can take and so we have four different values of P. We can use these four sets of values for $(\hat{}x_1;\hat{}x_2)$ and P to generate and solve four linear equations in c_0, c_1, c_2 and c_3. This approach can be generalized to gates with n inputs in the following manner.

Let $\rho_n = \{S_0, S_1, \ldots\ldots; S_{k-1}\}$ be the set of all subsets of $\{\hat{}x, \hat{}x_2\hat{}x_n\}$. Clearly, ρ_n has $k = 2^n$ elements. Define $\Pi(Si)$ as the product of the elements of S_i. We set $\Pi(\Phi) = 1$ For example,

ρ_3 = {Φ, {^x_1}, {^x_2}, {x_3}{^x_1,^x_2}{^x_2,^x_3}, {^x_3,^x_1}{^x_1^x_2,^x_3}, and_Π({^x_1,^x_2}) = x_1,^x_2.

Then we can write:

$$P(\hat{}x_1, \hat{}x_2, \hat{}x_n) = \sum_{i=0}^{k-10} ci\pi(Si) \quad (5)$$

Since (^x_1^x_2^x_n) and P(^x_1^x_2^x_n) can take on 2^n different values, we can substitute these values to obtain 2^n equations in ci which can then be solved in a straight forward manner to obtain a closed form expression for P(^x_1^x_2^x_n). For example consider Table I which shows leakage power values obtained from [10] for a 3-input NAND gate. Using the method detailed above we obtain the following equation[1].

P(^x_1^x_2^x_3) = 30.1+24.8·^x_1 + 24.6^x_2 + 25.^x_3 + 169.6. ^ x_1 ^ x_2 + 179.3 ^ x_1 ^ x_3 + 230.1 ^ x_2 ^ x_3 + 19.8 ^ x_1 ^ x_2^x_3 (6)

Table I

Input	Leakage (pW)	Input	Leakage (pW)
000	30.1	100	55.1
001	54.9	101	259.2
010	54.7	110	309.8
011	249.1	111	703.3

Typical Leakage Power Values for a 3-input Nand Gate.

Since we want to minimize leakage power, we express the objective of the ILP as minimize

$\sum_{j=1}^{N} P_j$ where Pj is the power dissipated by gate j of a circuit consisting of N gates.

B. I/O Constraints

To encode the relation between gate inputs and outputs, we introduce a set of constraints. Let the inputs of an input gate be ^x_1^x_2^x_n, and its output be ^y. For NOT, NAND and NOR gates respectively, we have the following relations:

$$\hat{}y = 1 - \hat{}x_1 \quad (7)$$

$$\hat{}y = 1 - \Pi \hat{}x_i \quad (8)$$

$$\hat{}y = 1 - \sum_i \hat{}X_i + \sum_{i,j} \hat{}X_i, \hat{}X_j + \ldots + (-1)^n \Pi \hat{}X_i \quad (9)$$

Similar constraints can be derived for other types of gates.

C. Path Delay Constraints

This set of constraints ensures that the the maximum NBTI degradation along each path is limited by L, the degradation limit Let us call any circuit path which could, depending on the input vector selected for use during sleep/standby mode, degrade so that its delay is greater than the degradation limit as a potentially critical path(PCP)[7].In this section we do not address the problem of how to select PCPs, but assume that they are already known. In this section we do not address the problem of how to select PCPs, but assume that they are already known. The delay of a gate after NBTI degradation depends on two factors: (1) the probability that the inputs of the gate are stressed during normal circuit operation and (2) the values at the inputs of the gate when the circuit is in standby/sleep mode. If the gate's input is a primary input, than we can directly control the value applied at the input of the gate. If it is an internal node, then its value depends on the value of the primary inputs in an indirect way. Define the nominal (undegraded) delay of a gate g as dg. Define the degraded gate delay of gate g on input values (^x_1, ^x_2............. ^x_n) as Dg(^x_1,^x_2............ ^x_n). In the rest of this subsection we show how to obtain closed form expression for Dg. Define p_0 (x_i) as the probability that input x_i is stressed during normal circuit operation, i.e. $p_0(x_i)$ = Pr{v(x_i) = 0}, where v(x_i) is the value of the input x_i during normal circuit operation. Note that v(x_i) is a random variable whose distribution is application dependent.

Although v(x_i) is itself not known, we can measure the value of $p_0(x_i)$ during circuit operation by conduction appropriate simulations like in [11]. We also define U as the circuit utilization, i.e. the fraction of time the circuit is not in standby/sleep mode. Then we can write the probability that the input x_i will be stressed ps(x_i) as:

$$Ps(x_i) = p_0(x_i) \cdot U + (1 - U) \hat{}\, x_i) \quad (10)$$

We can evaluate the $p_s(x_i)$for each input value ^x_i to obtain the degradation due to NBTI on each input of the gate. Selecting the maximum degradation among these gives us the degraded delay of the gate.

$$Dg(\hat{}x_1, \hat{}x_2, \hat{}x_n) = \max_i\{\Delta_d\, ps(x_i), t\} \quad (11)$$

Here ^x1 is the lsb, and ^x3 is the msb.

Dg gives the degraded delay of each gate as a function of its inputs. We can use the method outlined in Section III-A to obtain a closed form expression for Dg in terms of (^x_1,^x_2,^x_n).

Using this closed form expression for Dg for each gate g we can enumerate all the potentially critical paths and bound the sum of delays of the gates along the path to be less than the degradation limit. To be more precise for each potentially critical path P = (g_1, g_2.....g_k), we can write the constraint as

$$\sum_{i=1}^{k} Dg_i \leq L$$

D. Linearization Constraints

All the constraints we have derived so far use nonlinear functions, where some variables are the product of other

variables. We can easily convert these to linear functions by introducing a new variable and three additional constraints for each product variable. For example, consider the following constraint:

$$Z = 1 - xy \quad (12)$$

This can be linearized by introducing a new variable p representing the product of x and y and replacing the constraint (12)with the constaints in (13).

$$\begin{aligned} z &= 1 - p \\ p &\leq x \\ p &\leq y \\ x + y - p &\leq 1 \end{aligned} \quad (13)$$

It is easily verified that p is always the product xy when x, y $\in$ {0,1}. We use this method to convert all the nonlinear terms to linear terms in the constraints presented in the previous sections.

Table II
Results of Experiments on ISCAS'85 Benchmarks

Circuit	RND leakage max(μW)	RND leakage min(μW)	ILP leakage	ILP degradation	Worst case
c880	0.32	0.29	0.29	10%	16%
c1908	0.71	0.68	0.68	10%	16%
c3540	1.55	1.50	1.51	11%	16%
c432	0.14	0.12	0.12	11%	17%

4. EVALUATION

A. Methodology

We developed a C++ simulator that generates the ILP model which takes as input a synthesized netlist, estimates the probability that a given input is stressed during normal circuit operation and generates the constraints and the objectives of the ILP. Since NBTI degradation is circuit as well as input dependent, it is not possible to use a single degradation limit for all circuits. Therefore,we developed another C++ tool that generates a large number (e.g.20;000) random vectors and searches for the vector with minimum NBTI degradation among these. We then select the degradation limit as L min + _where Lmin is the minimum of the degraded delays and _is a small constant less than 0 :1% of the maximum circuit delay that leaves some "slack" to find an input vector with lesser leakage power. Like in [9, 10] we assume that circuit utilization is U = 10%.

5. RESULT

Table III shows the results of our experiments on some of the ISCAS '85 benchmarks. To provide a reference for comparison, we show the minimum and maximum leakage power values obtained when searching over a large number (e.g.20;000) random input vectors. While this method can uncover some random vectors with low leakage power, it is difficult to find a vector that simultaneously minimizes leakage power and NBTI degradation. The results of the random search algorithm are shown in the first two columns of table III. The results of our ILP solution are shown in the third and fourth columns. We can see that the ILP solution is able to find a single input vector that minimizes both leakage power and NBTI degradation. The final column shows that the input vector derived using the ILP solution is significantly better than the worst case degradation

6. CONCLUSION

In this paper we introduced an ILP formulation for determining an input vector that minimizes leakage power while simultaneously constraining the maximum NBTI degradation due to that vector. Our results show that these leakage vectors are within 1% of the minimum leakage obtained by searching the input vector space and reduce the NTBI degradation by 5.75% of the maximum circuit delay as compared to the worst case. We also introduced two new algorithms for selecting potentially critical paths that produce order of magnitude reductions in the number of critical paths selected as compared to previous work.

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